

PATENTS
174/079ReIN THE UNITED STATES PATENT AND TRADEMARK OFFICE
REISSUE APPLICATION

Application for

Reissue of Patent No.: 5,970,255

Issued : October 19, 1999

Patentee/

Reissue Applicants : Nghia Tran, Ying Xuan Li, Janusz
Balicki, and John CostelloFor : SYSTEM FOR COUPLING PROGRAMMABLE
LOGIC DEVICE TO EXTERNAL CIRCUITRY
WHICH SELECTS A LOGIC STANDARD AND
USES BUFFERS TO MODIFY OUTPUT AND
INPUT SIGNALS ACCORDINGLY

Assignee : Altera Corporation

Box REISSUE

Hon. Commissioner for Patents
Washington, D.C. 20231October 19, 2001
New York, NY 10020INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97,
applicants wish to call the attention of the Examiner to the
following references:

U.S. patents	Re 34,808 Hsieh
	4,032,800 Druscher et al.
	4,472,647 allgood et al.
	4,527,079 Thompson
	4,625,129 Ueno
	4,783,607 Hsieh



4,791,312 Weick
 4,797,583 Ueno et al
 4,820,937 Hsieh
 4,879,481 Pathak et al.
 4,933,577 Wong et al
 4,970,410 Matsushita et al.
 4,975,602 Nhu
 4,987,319 Kawana
 4,994,691 Naghshineh
 4,999,529 Morgan, Jr. et al.
 5,023,488 Gunning
 5,028,821 Kaplinsky
 5,034,634 Yamamoto
 5,132,573 Tsuru et al.
 5,151,619 Austin et al.
 5,235,219 Cooperman et al.
 5,282,271 Hsieh et al.
 5,300,835 Assar et al.
 5,311,080 Britton et al.
 5,317,210 Patel
 5,332,935 Shyu
 5,374,858 Elmer
 5,428,305 Wong et al.
 5,428,800 Hsieh et al.
 5,534,794 Moreland
 5,534,798 Phillips et al.
 5,589,783 McClure
 5,612,637 Shay et al.

EPO Applications 0 358 501
 0 426 283 B1
 0 544 461 A2
 0 608 515 A1
 0 616 431 A1

Japan Applications 01-274512
 02-013124
 02-161820
 04-223617

B.A. Chappell, et al., "Fast CMOS ECL Receivers with 100mV Worst-Case Sensitivity" IEEE Journal of Solid-State Circuits, Vol. 23, No. 1, February 1988, pp. 59-66.

F. Claude, "Cross-boundry PLDs", Semiconductor Currents, June 1991, pp. 9-10.

Carlo Guardiani, et al., "Applying a submicron mismatch model to practical IC design" IEEE 1994 Custom Integrated Circuits Conference, 1994, pp. 297-300.

Bill Gunning, et al., "A CMOS Low-Voltage-Swing Transmission-Line Transceiver" IEEE International Solid-State Circuits Conference, 1992, pp. 58-59.

Andrew Haines, "Field-programmable gate array with non-volatile configuration", Microprocessors and Microsystems, Vol. 13, No. 5, June 1989, pp. 305-312

H.I. Hanafi, et al., "Design and Characterization of CMOS Off-Chip Driver/Receiver with Reduced Power-Supply Disturbance", IEEE Journal of Solid-State Circuits, Vol. 27, No. 5, May 1992, pp. 783-785.

"IEEE 1194.1 BTL-Enabling Technology for High Speed Bus Applications", June 1992, pp. 1-5.

K. Knack, "Debunking High-Speed PCB Design Myths", ASIC & EDA, July 1993, pp. 12-26.

M.J.M. Pelgrom, et al., "A 3/5 V Compatible I/O Buffer", IEEE Journal of Solid-State Circuits, Vol. 30, No.7, July 1995, pp. 823-825.

M.J.M. Pelgrom, et al., "Matching Properties of MOS Transistor", IEEE Journal of Solid-State Circuits, Vol. 24, No.5, October 1989, pp. 1433-1440.

B. Prince, et al., "ICS going on a 3-V diet", IEEE Spectrum, May 1992, pp. 23-25.

A.L. Roberts, "Session XIX: High Density SRAMs", IEEE International Solid-State Circuits Conference, February 1987, pp. 252-254.

R. Senthinathan, "Application Specific CMOS Output Driver Circuit Design Techniques to Reduce Simultaneous Switching Noise", IEEE Journal of Solid-State Circuits Conference, Vol. 28, No. 12, December 1993, pp. 1383-1388.

R. Senthinathan, "Simultaneous Switching Ground Noise Calculation for Packaged CMOS Devices", IEEE Journal of Solid-State Circuits Conference, Vol. 26, No. 11, November 1991, pp. 1724-1728.

M. Ueda, "A 3.3V ASIC for Mixed Voltage Applications with Shut Down Mode", IEEE Custom Integrated Circuits Conference, 1993, pp. 25.5.1 - 25.5.4.

S. H. Voldman, "ESD Protections in a Mixed Voltage Interface and Multi-Rail Disconnected Power Grid Environment in 0.50 and 0.25 Channel Length CMOS Technologies", EOS/ESD Symposium, pp. 3.4.1 - 3.4.10, 1994.

T.T. Vu., "A Gallium Arsenide SDFL Gate Array with On-chip RAM", IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 1, February 1984, pp. 10-22.

J. Williams, "Mixing 3-V and 5-V Ics", IEEE Spectrum, March 1993, pp.40-42.

These references are also listed on the attached Form PTO-1449, and copies of them are enclosed.

Consideration of the foregoing in relation to this patent application is respectfully requested.

Respectfully submitted,



Michael E. Shanahan
Registration No. 43,914
Attorney for Applicants
and Assihnee
FISH & NEAVE
Customer No. 1473
1251 Avenue of the Americas
New York, New York 10020
Tel.: (212) 596-9000